An Extremely Small 26 GHz Monolithic Image-Rejection Mixer Without DC Power Consumption

Akira Minakawa and Tetsuo Hirota

Abstract— **This paper describes several design methods for an extremely small 26 GHz monolithic image-rejection mixer. The bias dependence of the drain LO injection mixer is also investigated. Consequently, it was found that there exists an optimum bias point for minimum conversion loss, and the mixer performed well even with zero drain bias voltage. The mixer is fabricated using a uniplanar technique. It consists of drain LO injection mixers, a reduced-size branch-line hybrid, and a Wilkinson divider with a compact layout. The chip measures only 1.6 mm × 1.3 mm, which is the smallest among those reported.**

I. Introduction

THE small size and repeatable performance of monolithic microwave integrated circuits (MMICs) have a strong impact on reducing the cost and size of all microwave equipment. To enhance radio system equipment performance, microwave radio systems often use an image-rejection mixer as a frequency down converter. The image rejection technique using a phasing technique [1] is extremely practical in MMICs because the image rejection filters are difficult to implement on a chip due to the MMICs' low Q property. Brady *et al.* [2] have reported a Ka-band phasing-type image-rejection mixer, but as is common in phasing-type image-rejection mixers, the circuit is rather large. These mixers must be miniaturized to reduce their cost. In addition, conventional FET mixers consume dc power. This is undesirable in systems where reducing power consumption is urgent. In general, there are two types of single-gate FET mixer configurations. One type is the gate mixer [3], [4], and the other type is the drain LO injection mixer [5], [6]. The gate mixers are large because they need a balanced configuration or filters to provide RF and LO signal isolation. Therefore, in this paper, a drain LO injection mixer is adopted as a unit mixer from the viewpoint of miniaturization. There have been several papers analyzing FET mixers [3], [7], and the analysis of a drain LO injection mixer has also been reported [8]. However, in these works, the drain bias dependence of the mixer was not considered.

This paper describes size reduction techniques for an image-rejection mixer and analyzes a drain LO injection mixer. The image-rejection mixer incorporates drain LO injection mixers, a reduced-size branch-line hybrid, and a Wilkinson divider with a compact layout. A uniplanar technique [9] is also employed for effective compact layout. By using these techniques, the chip size of the 26 GHz monolithic image-rejection mixer was reduced to only 1.6 mm × 1.3 mm, which is the smallest among those reported. Our analysis of the drain LO injection mixer, when the drain bias is changed, indicated that there exists an optimum bias point for minium conversion loss and that this mixer can be operated even when drain voltage is not applied. This fact is very beneficial when this mixer is applied to, for instance, mobile systems where the reduction of power consumption is urgent.

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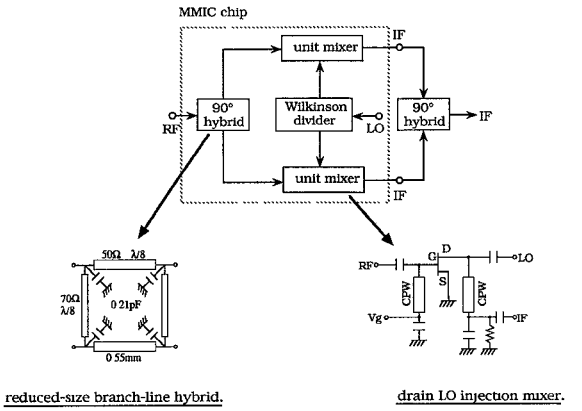

Fig. 1. A schematic diagram of the image-rejection mixer.

II. Size Reduction Techniques for the Image-Rejection Mixer

A. Basic Circuit Configuration of the Image-Rejection Mixer

A schematic diagram of the image-rejection mixer is shown in Fig. 1. The mixer consists of two drain LO injection unit mixers, a reduced-size branch-line hybrid circuit for the RF input signal, and a Wilkinson divider for the LO signal. The two IF output signals are combined with an external 90° hybrid. The input RF signal is split into quadrature signals by the reduced-size 90° hybrid described in the next section. After splitting they are fed to the FET gates. The LO signal is split in phase by a Wilkinson divider and fed to the drains. The two down-converted quadrature IF signals are derived from the two unit mixers.

B. The 90° Hybrid and Wilkinson Divider

Since a large area of the image-rejection mixer is take up by a 90° hybrid circuit and an in-phase power divider in conventional technique, it is important to reduce their size as well. To accomplish this, we use combinations of short length high-impedance coplanar waveguides (CPWs), shunt lumped capacitors and closely spaced meander CPWs.

A quarter-wavelength transmission line with characteristic impedance Z_0 can be equivalently converted to a shortened transmission line, and shunt lumped capacitors connected at both ends of the line. Using a size reduction method [10], we set

$$Z = Z_0/\sin\theta$$
$$\omega C = (1/Z_0)\cos\theta$$

where Z_0, Z, θ, and C are the characteristic impedance of the quarter-wavelength line in an original branch-line hybrid, the characteristic impedance of the shortened line, the electrical length of the shortened line, and the lumped capacitance for the capacitor loaded line, respectively. ω is the angular frequency. From these two equations, we obtain the values of the characteristic impedances, the transmission line lengths, and the capacitance of the shunt capacitor, as shown in Fig. 1. This hybrid is scaled down to about one-fourth that of a conventional (quarter-wavelength) branch-line hybrid. In addition, the Wilkinson divider uses closely spaced coplanar waveguides with low-coupling properties to reduce the chip size. It is only 0.5 mm × 0.4 mm.

III. Experiments on Unit Mixer with Drain LO Injection

A. Operating Principle of Drain LO Injection Mixer

This mixer makes use of the nonlinearity of drain resistance when a large LO signal is applied to the drain. The time dependence of drain resistance, when the drain bias voltage is changed, is shown in Fig. 2. When the drain bias voltage is changed, the nonlinearity effect is also changed. For example, in Fig. 2(a), drain resistance R_d is almost constant for time t ($R_d = R_{ds}$), where R_{ds} is drain resistance for a saturated drain current. Similarly, in Fig. 2(c), $R_d = R_{du}$ for time t, where R_{du} is drain resistance for unsaturated drain current. On the other hand, in Fig. 2(b), R_d varies between R_{du} and R_{ds} for time t. Therefore, drain resistance is modulated by the large LO signal, and nonlinearity can be expected. An optimum point of conversion gain (or loss) exists within region (b) for V_d. When a large LO signal is applied to the drain, this relation can be maintained even when the drain bias voltage is set to zero. Therefore, this drain mixer can be operated even when the drain voltage is zero.

The magnitude of nonlinearity is dependent on the bias voltage and the LO signal input power. In this paper, we experimentally show the optimum condition of gate and drain bias voltage. Fig. 3 shows the measured minimum conversion loss as a function of gate (V_{gs}) and drain (V_{ds}) bias voltage. This measurement obtains V_{ds} when the conversion loss is the minimum value for a fixed V_{gs}, provided that this measurement is carried out for only an FET (no matching circuit). From this

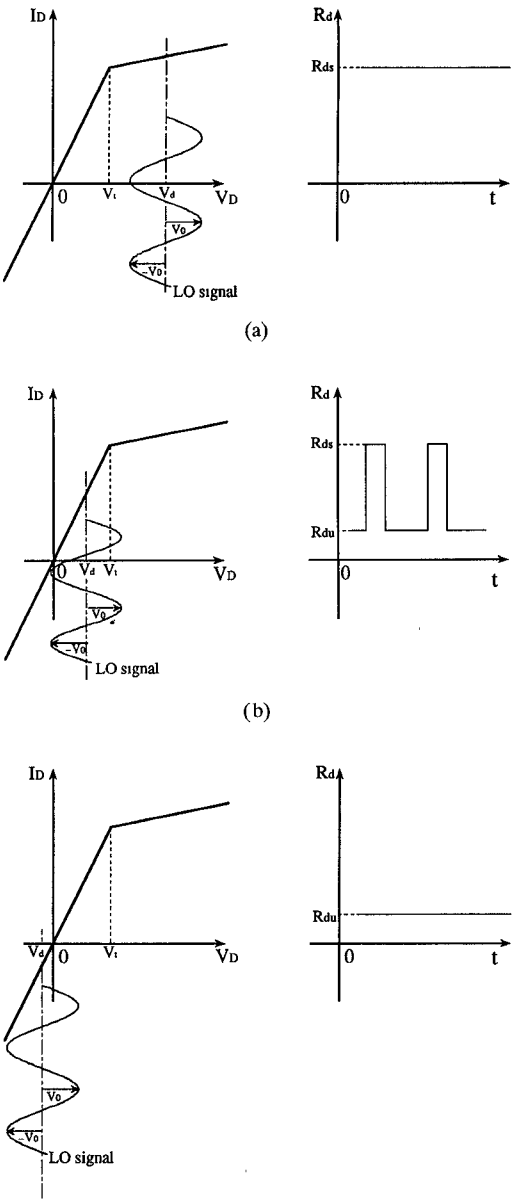

Fig. 2. Three examples of time dependence of drain resistance when drain voltage is changed. (a) $V_d - V_0 > V_t$. (b) $V_d + V_0 > V_t$ or $V_d - V_0 < V_t$. (c) $V_d + V_0 < V_t$.

figure, it is found that the bias point for minimum conversion loss is $V_{gs} = -0.55$ V and $V_{ds} = 0.17$ V. The conversion gain is given by [8]

$$G_c = \frac{1}{4}\left(\frac{g_m}{\pi\omega C_{gs}}\right)^2 \frac{R_d}{R_g}$$

where

g_m : the transconductance;
C_{gs} : the gate-source capacitance;
R_g : the gate resistance.

For our FET, $C_{gs} = 0.5$ pF, $R_g = 3\ \Omega$, $R_d = 200\ \Omega$, and $g_m = 30$ mS. This results in a conversion gain of $G_c = -6$ dB at 26 GHz.

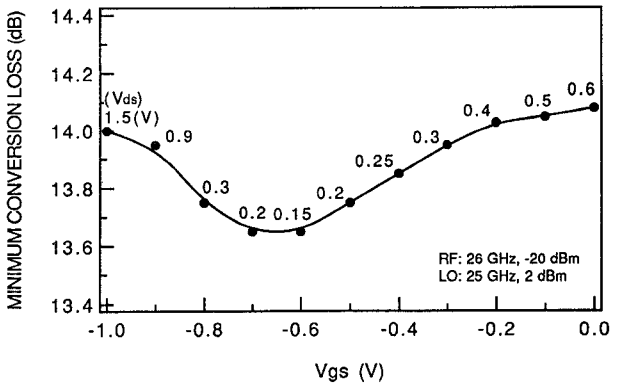

Fig. 3. Measured minimum conversion loss as a function of gate bias voltage and drain bias voltage.

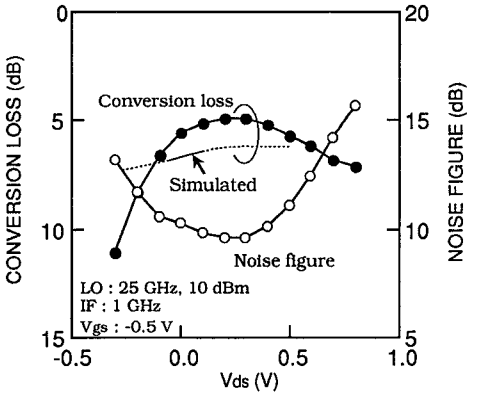

Fig. 4. Conversion loss and noise figure versus drain bias voltage of the unit mixer.

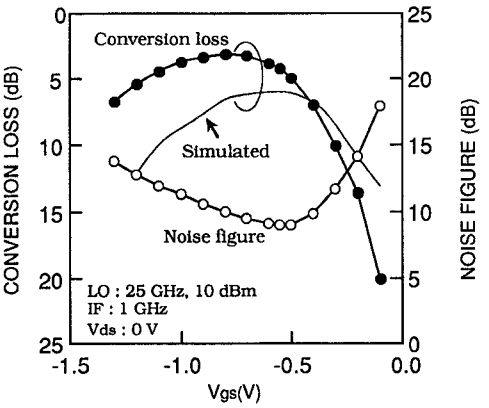

Fig. 5. Conversion loss and noise figure versus gate bias voltage of the unit mixer.

B. Design Method

The RF and LO port impedance matching is done with simple matching circuits composed of shunt coplanar waveguide stubs and series capacitors. We carried out fitting with respect to S11, S22, and S21. The circuit parameters in the mixer circuit were primarily determined using the linear circuit simulator SUPER-COMPACT. Then, the conversion loss simulation was performed by the nonlinear circuit simulator SPICE. The FET model of SPICE, which we used, also had external gate-source capacitance (C_{gs}) and drain-source capacitance (C_{ds}).

C. Performance of Unit Mixer

The conversion loss and noise figure dependence on drain bias voltage of the unit mixer with drain LO injection are shown in Fig. 4. The optimal conversion loss and noise figure were obtained at a drain voltage (V_{ds}) of about 0.2 V. The measured results show good performance even at a drain bias voltage of zero, which is consistent with the theoretical consideration described in the previous section. This means that the drain LO injection mixer does not need drain bias and has no dc power consumption. In addition, the chip size is smaller because the drain bias circuit is not necessary. In this figure, since our FET model was optimized to fit the measured parameters in the vicinity of $V_{ds} = 0$, the measured conversion loss and the simulated values do not agree except for that region. Fig. 5 shows the conversion loss and noise figure dependence on the gate bias voltage. With a gate bias voltage (V_{gs}) of -0.5 V, the noise figure is at the minimum. The IF output power and the 3rd-order intermodulation (IM_3) output level versus RF input power are measured. The intercept point is about 13 dBm. It was confirmed that the simulated output power using SPICE agreed well with the measured values.

IV. Performance of the Image-Rejection Mixer

Fig. 6 shows a photograph of the fabricated image-rejection mixer. In this image-rejection mixer, the unit mixers are drain LO injection mixers. The 90° hybrid circuit for the RF input signal is a reduced-size branch-line hybrid. The in-phase LO power divider is a Wilkinson divider with quarter-wavelength transmission lines. The whole chip measures only 1.6 mm × 1.3 mm, which is the smallest chip size in the 26 GHz bands [2], [11], [12], RF frequency dependence of the conversion loss and image rejection ratio are shown in Fig. 7. The RF frequency is the upper-side-band frequency for the LO frequency. The IF frequency was set at 1 GHz. In the 25–26 GHz RF frequency band, a conversion loss of 6 dB and an image rejection ratio of more than 25 dB were obtained. The conversion loss includes the loss of the reduced-size hybrid and the external IF hybrid.

V. Conclusion

An extremely small 26 GHz image-rejection mixer has been designed and fabricated. An examination of the bias dependence of the drain LO injection mixer showed that there exists an optimum bias point for minimum conversion loss. It was also found that the mixer performed well even with zero drain bias voltage. The integrated image-rejection mixer employs drain LO injection mixers without dc power consumption as unit mixers, a reduced-size branch-line hybrid as a quadrature hybrid, and a Wilkinson divider with a compact layout. It showed an excellent image rejection ratio of more than 25 dB with a chip size of only 1.6 mm × 1.3 mm. The newly developed mixer will help to reduce the cost and size of microwave radio systems.

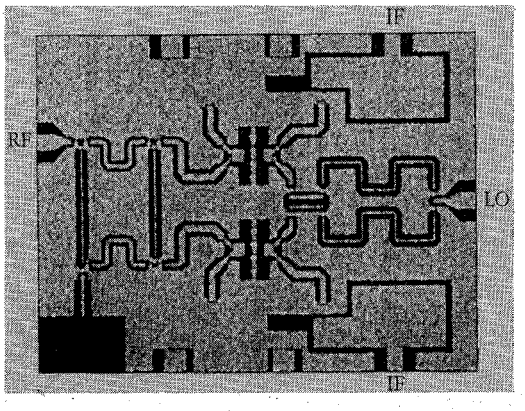

Fig. 6. Photograph of the 26 GHz image-rejection mixer.

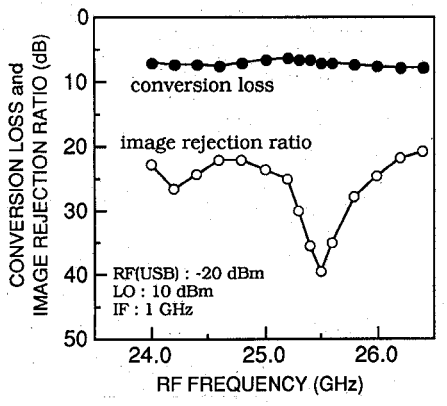

Fig. 7. Conversion loss and image rejection ratio versus RF frequency.

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Akira Minakawa, photograph and biography not available at the time of publication.

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